



TESSERA 3.3-018 CONT CONT II CONT II CONT II PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of :
Khandros, et al. : Group Art Unit 2815
Appln. No. 09/691,807 : Examiner: Sheila Clark
Filed: October 19, 2000 : Confirmation No. 5389
For: STACKED CHIP ASSEMBLY : Dated: July 10, 2002
X

Commissioner For Patents
Washington, D.C. 20231

TRANSMITTAL OF FORMAL DRAWINGS

Sir:

Enclosed herewith are twenty (20) sheets of formal drawings for filing in connection with the above-identified application. The formal drawings are submitted in order to correct the informalities listed in form PTO-948.

In the event there are any fees due and owing in connection with this matter, please charge same to our Deposit Account No. 12-1095.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231 on July 10, 2002.

(Signature)

Arnold H. Krumholz

Typed or Printed Name of Person Signing Certificate

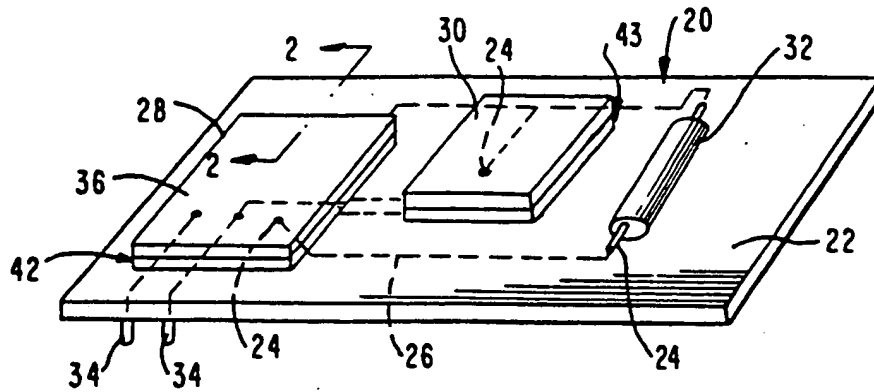


FIG. 1

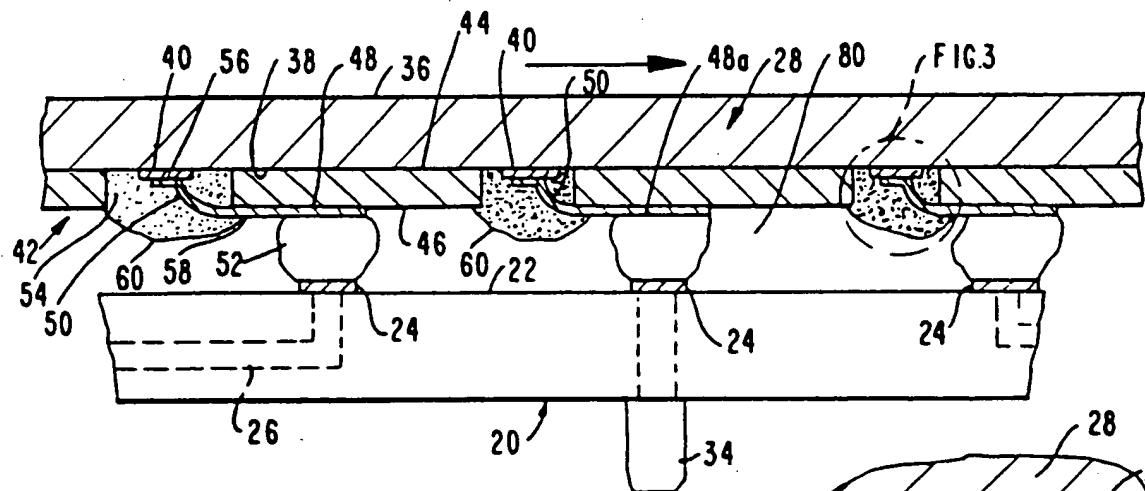


FIG. 2

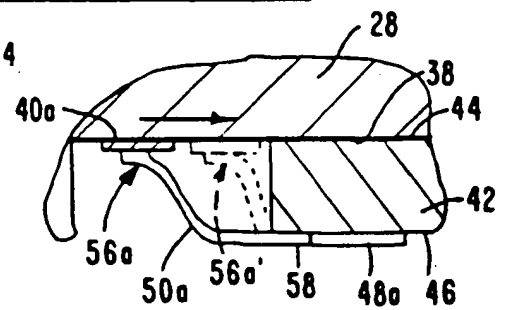


FIG. 3

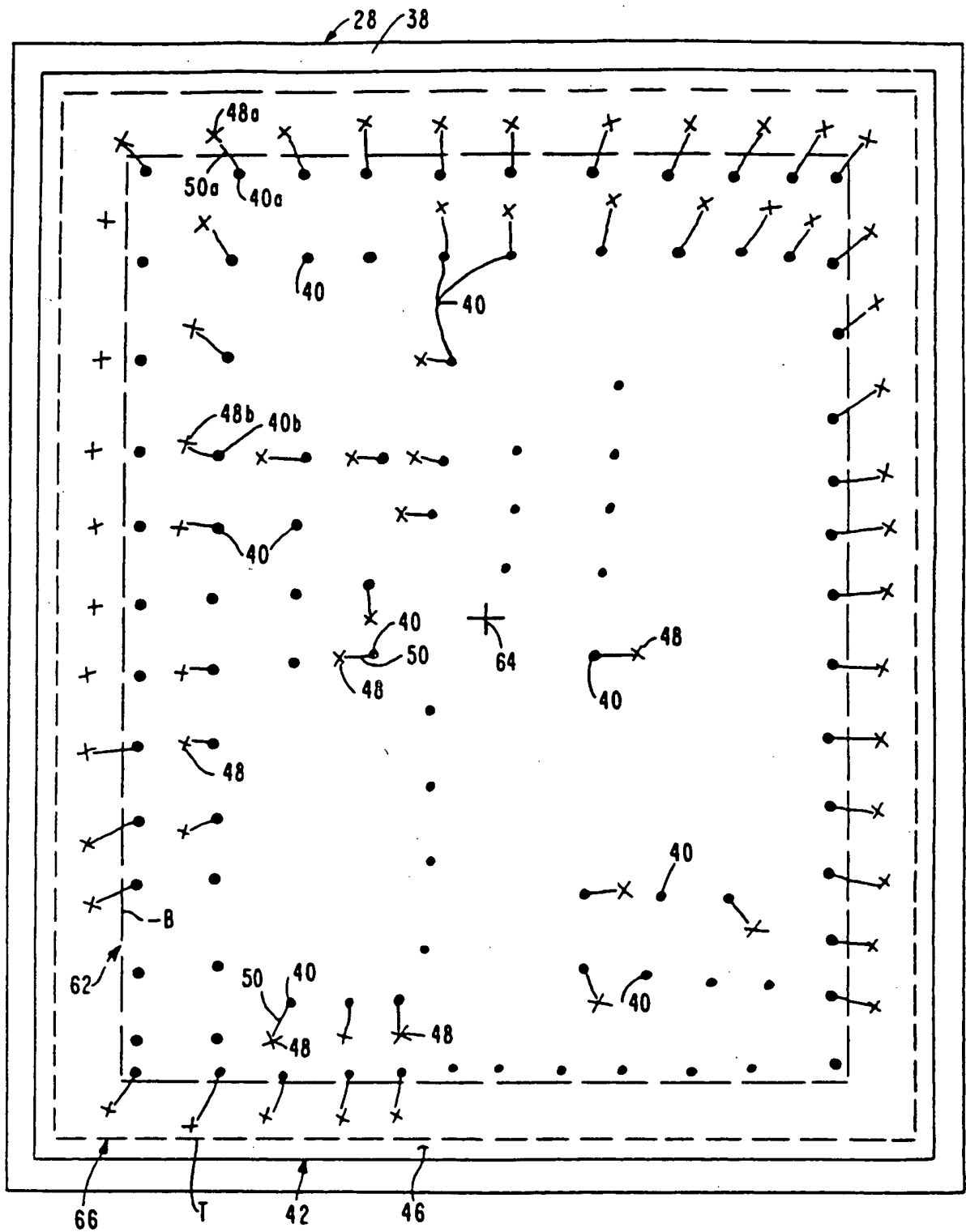


FIG. 4

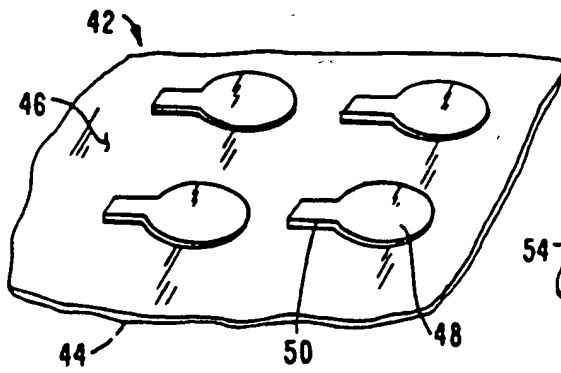


FIG. 5A

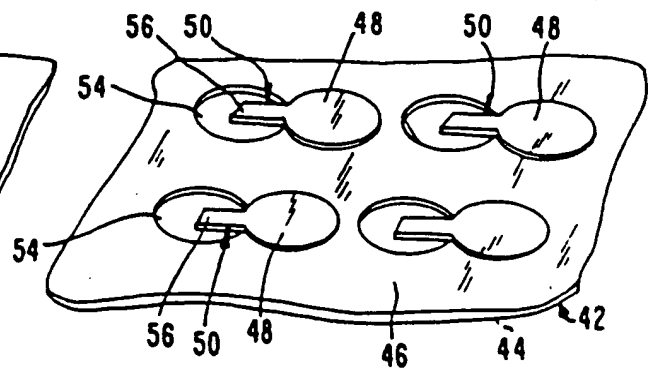


FIG. 5B

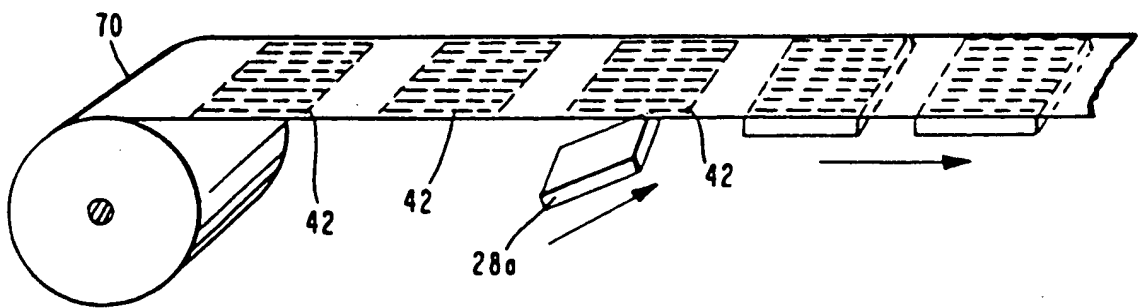


FIG. 6

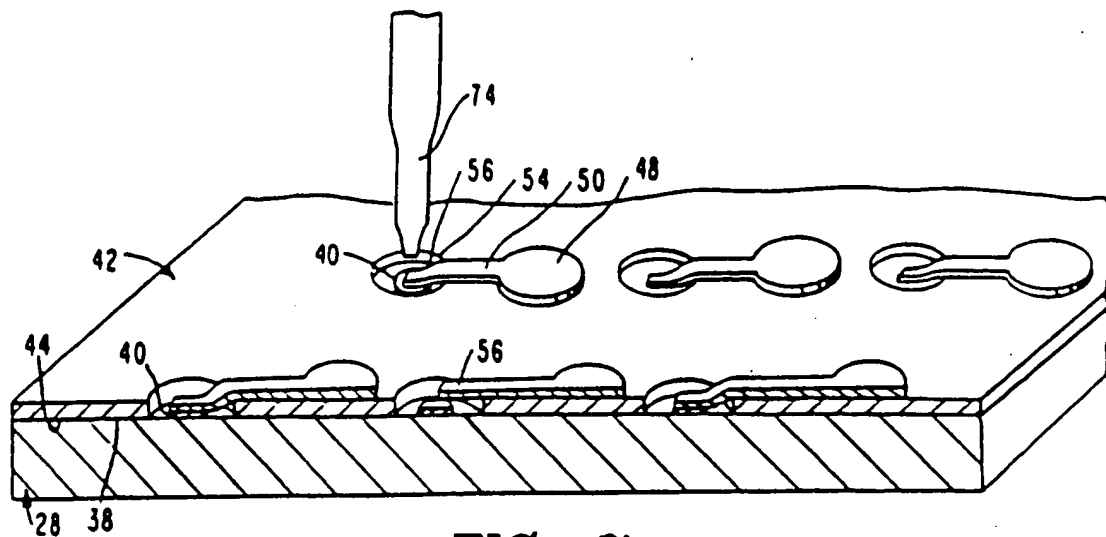


FIG. 7

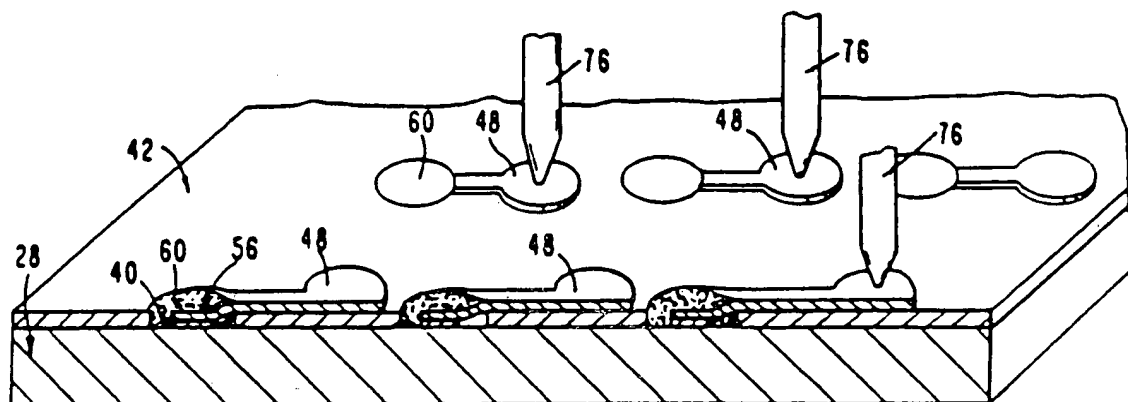


FIG. 8

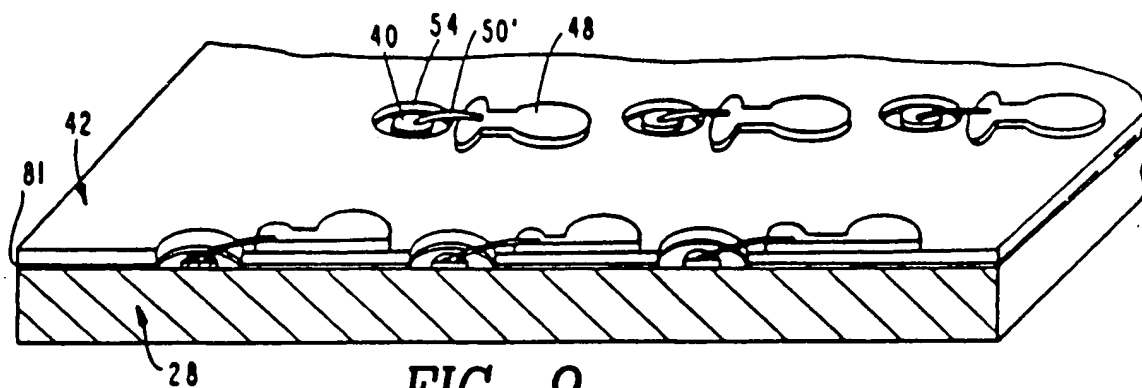


FIG. 9

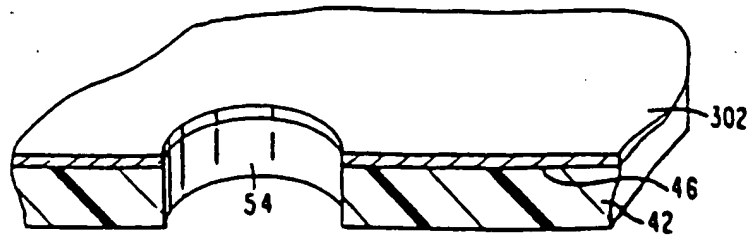


FIG. 10A

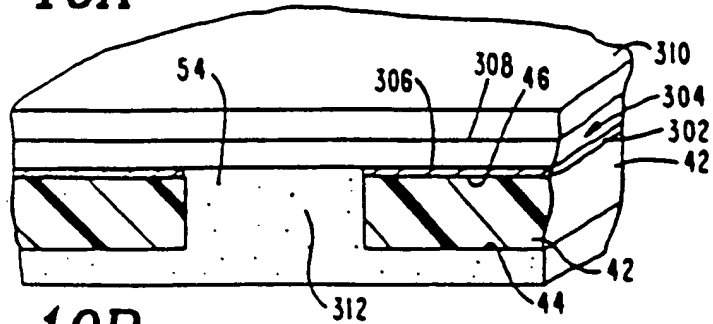


FIG. 10B

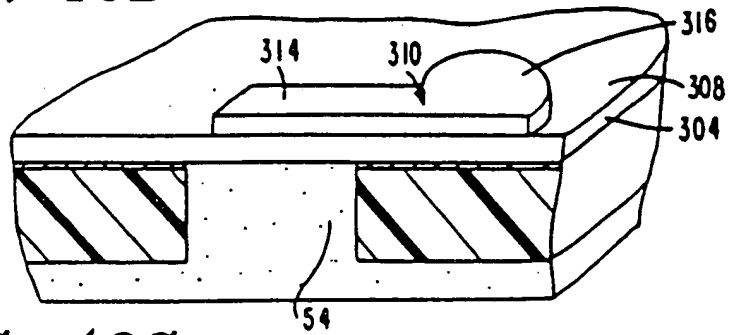


FIG. 10C

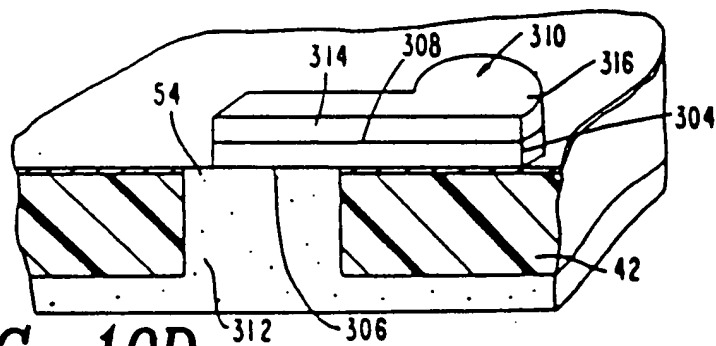


FIG. 10D

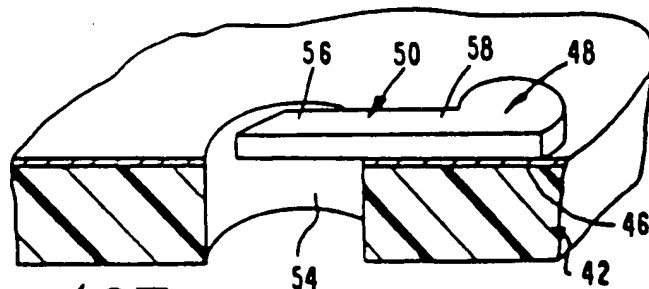


FIG. 10E

FIG. 11

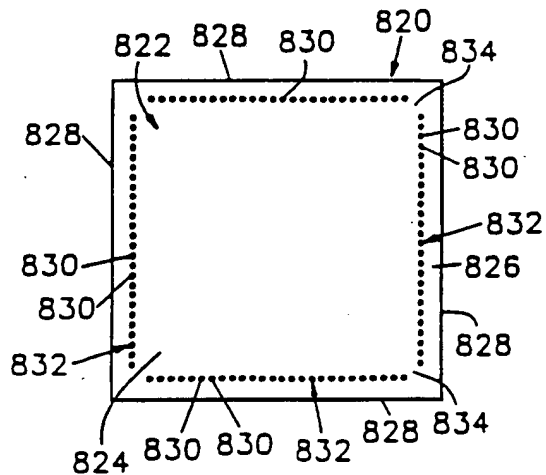


FIG. 12

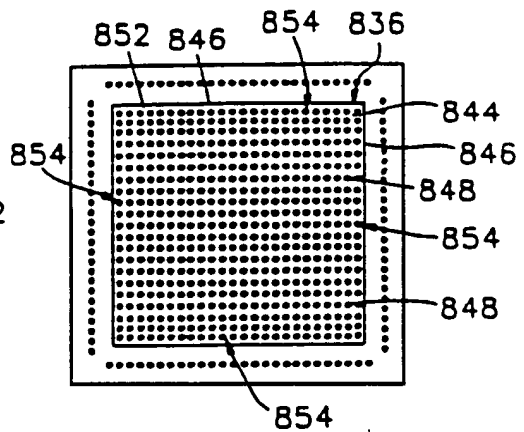


FIG. 17

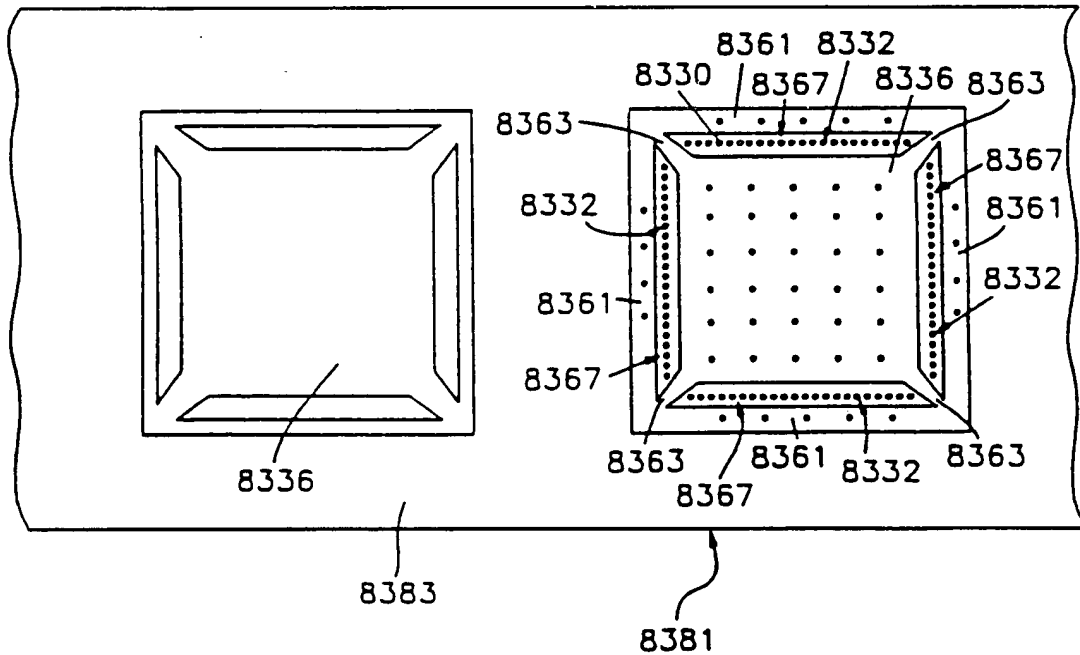


FIG. 13

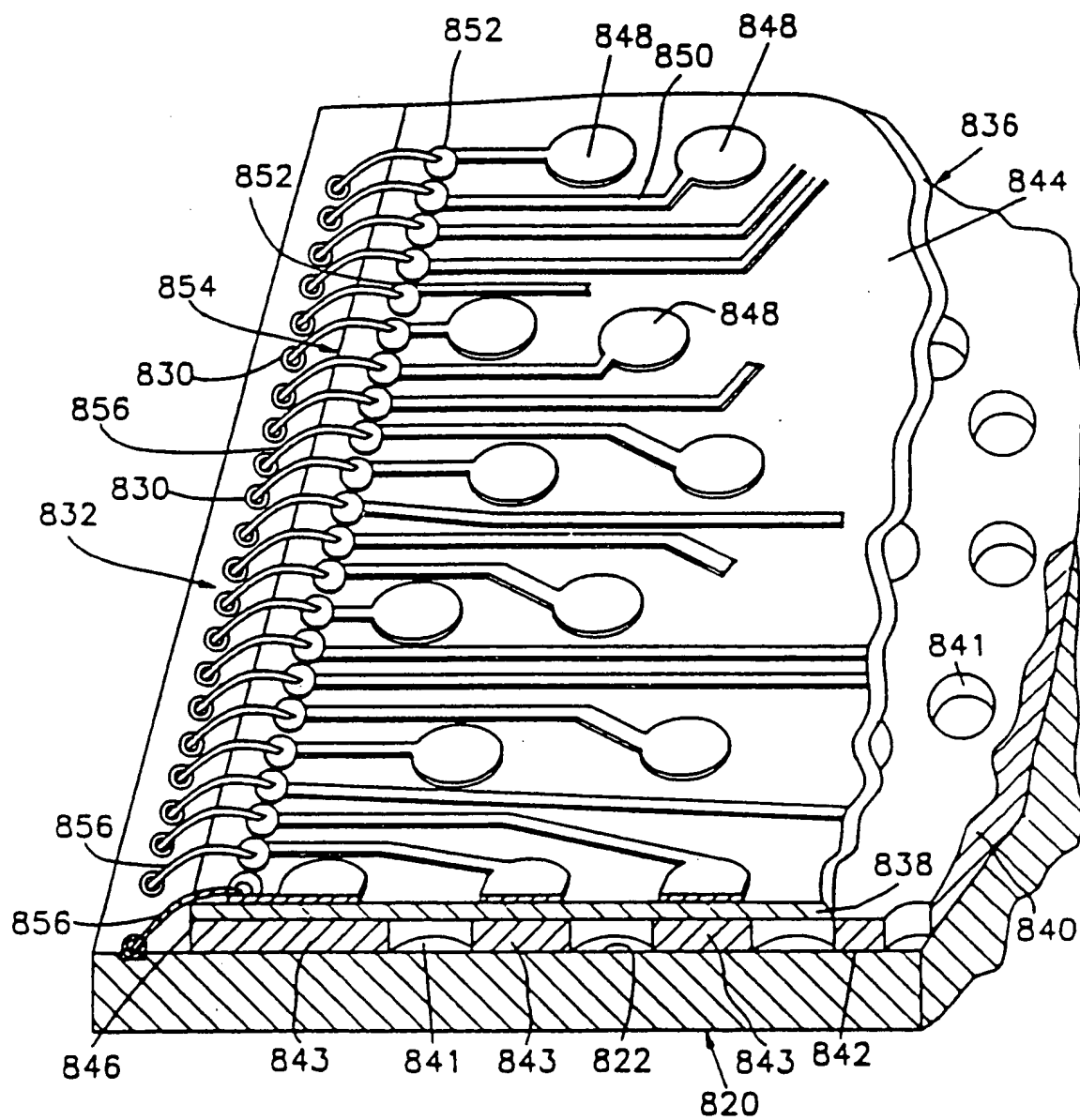


FIG. 14

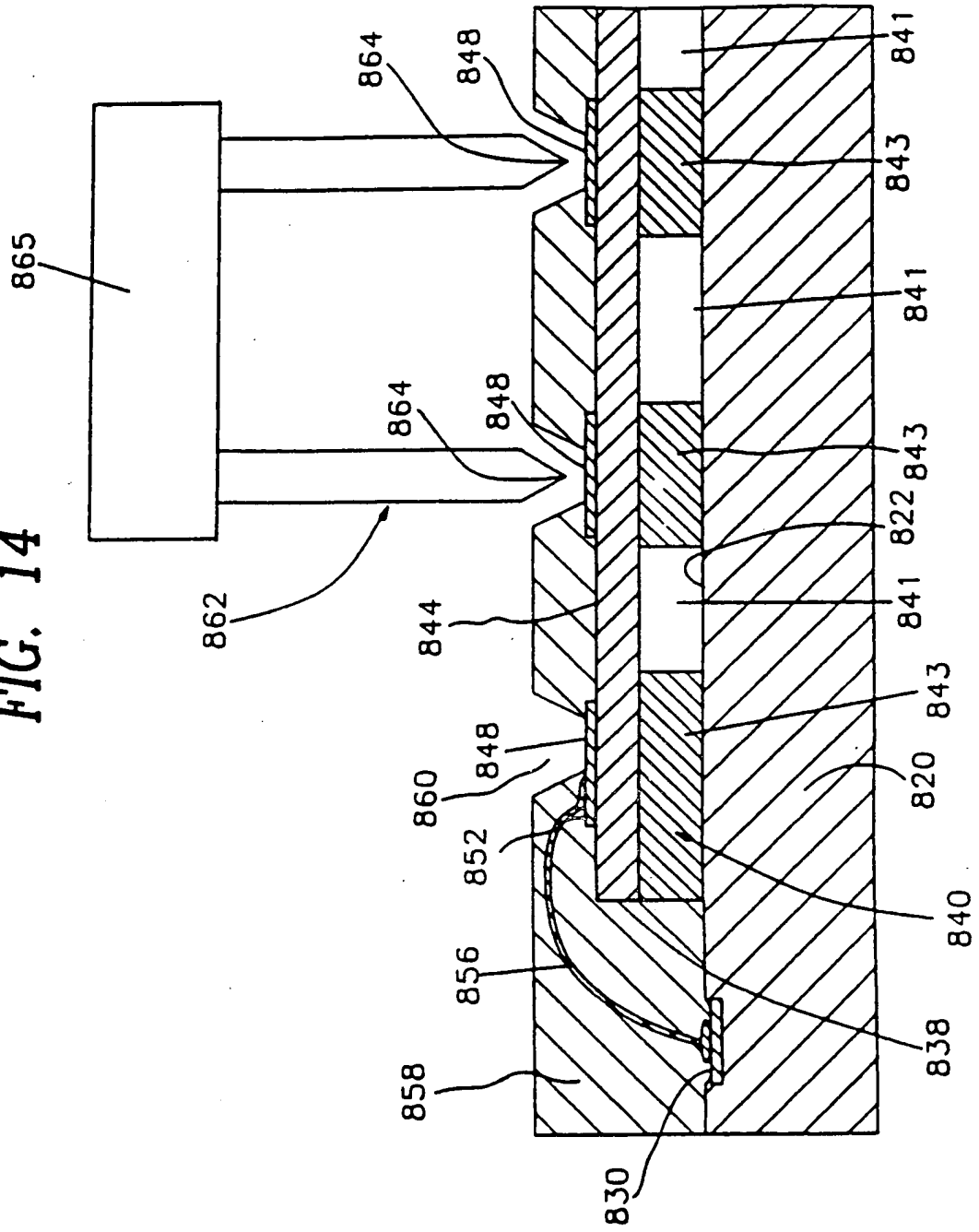


FIG. 15

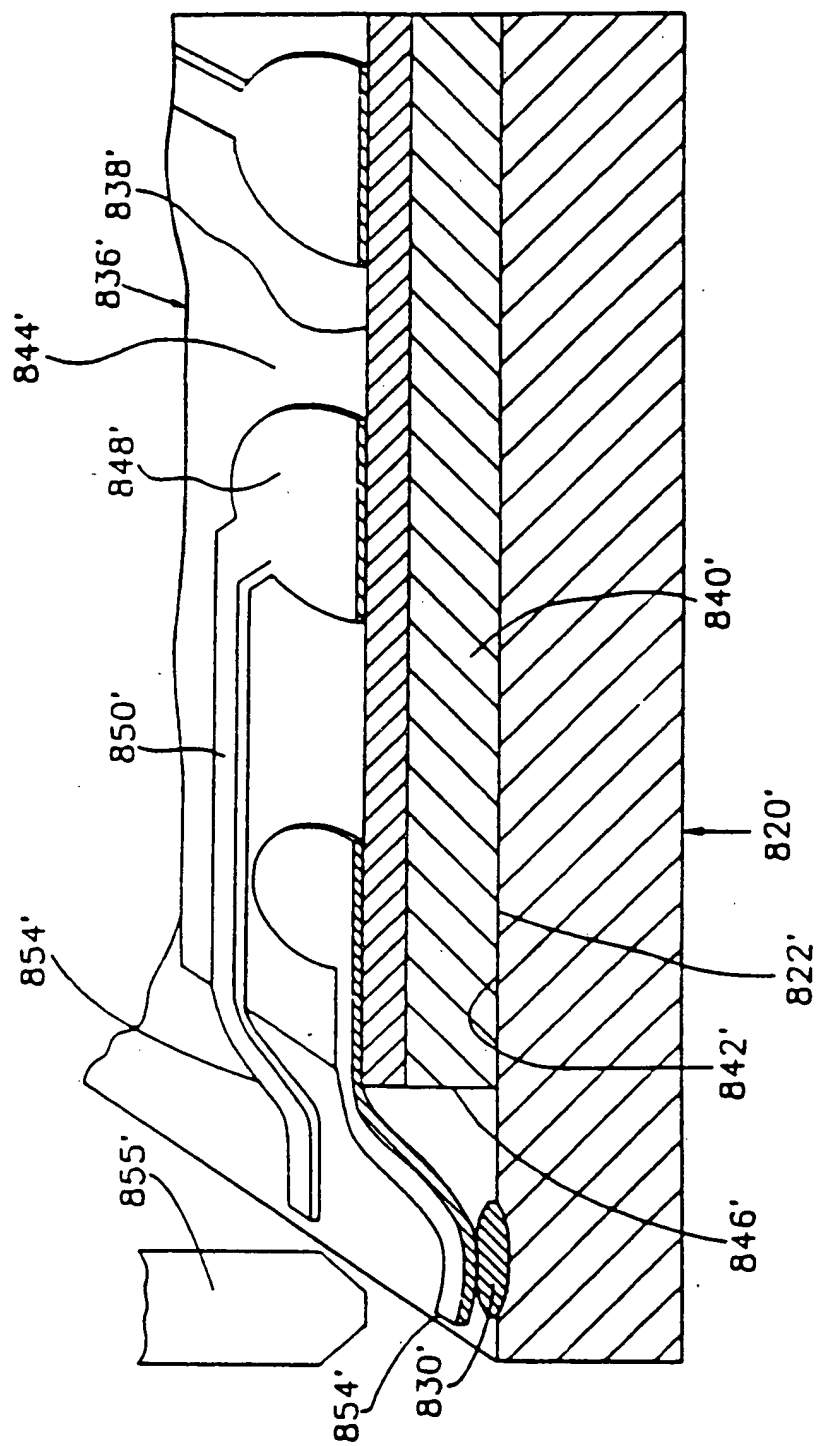


FIG. 16

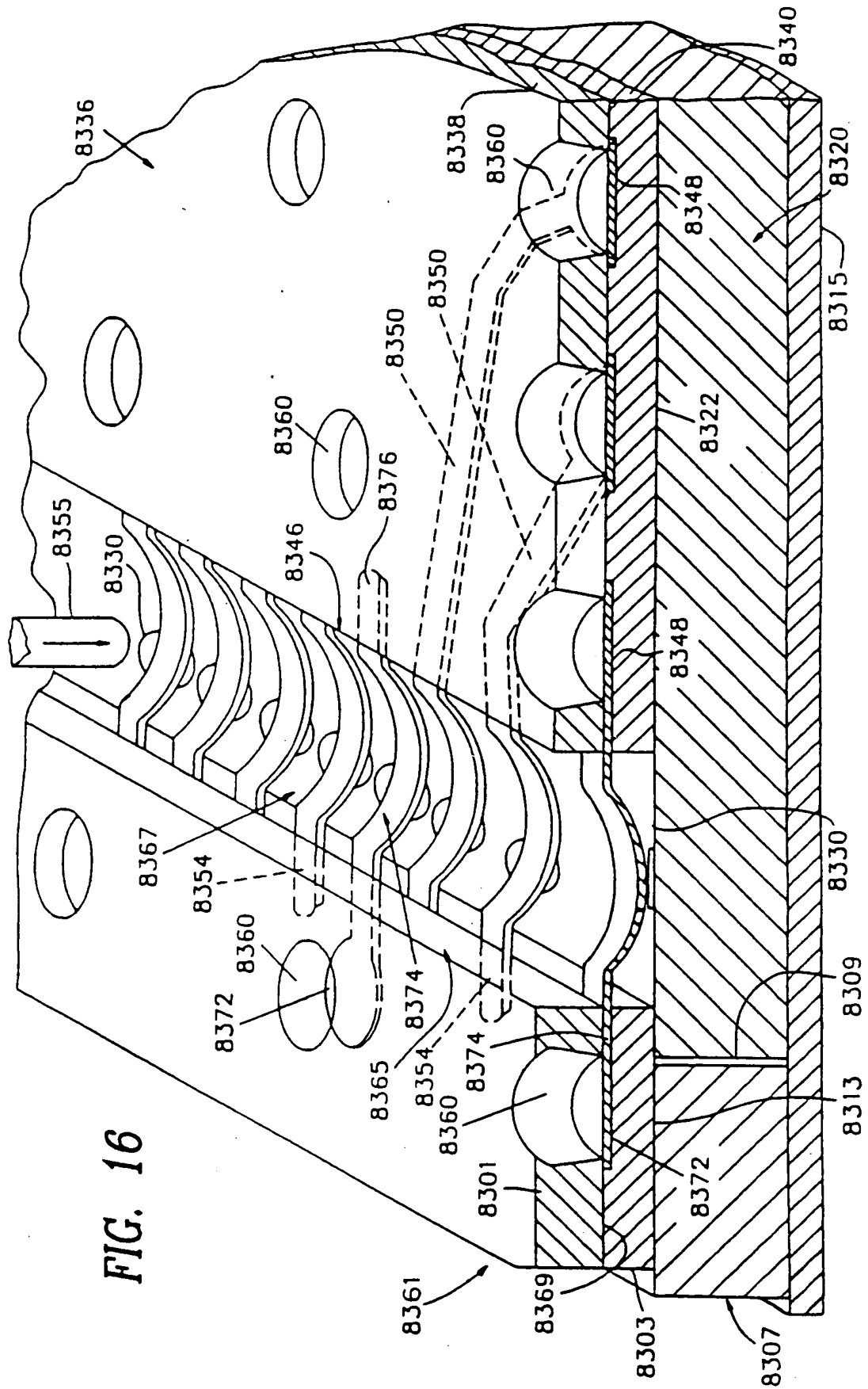


FIG. 18

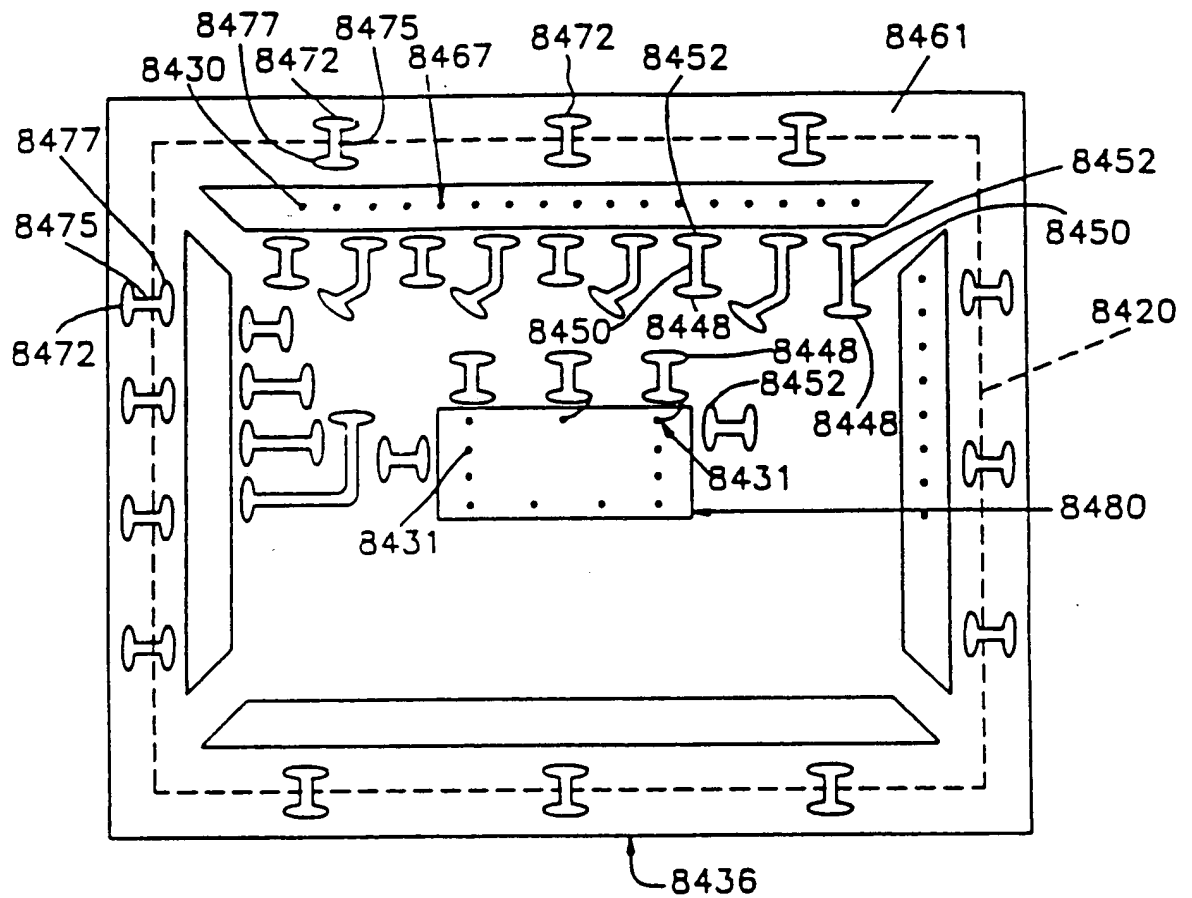
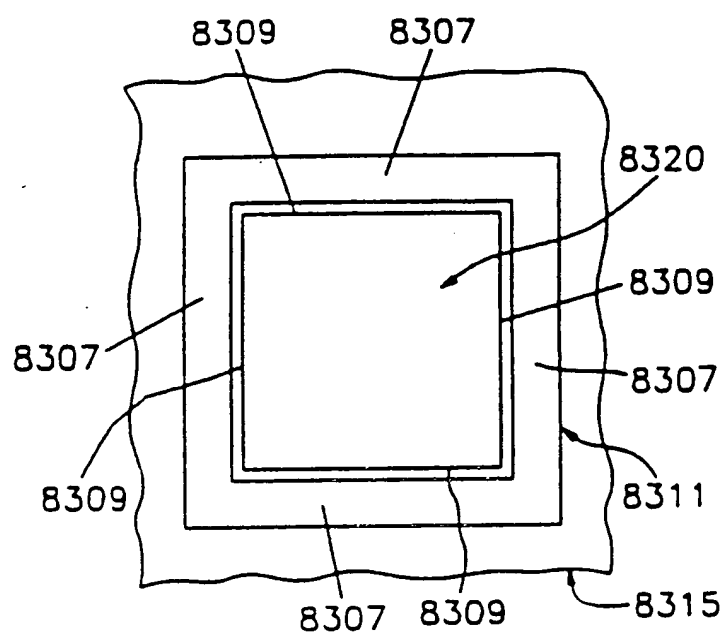


FIG. 19



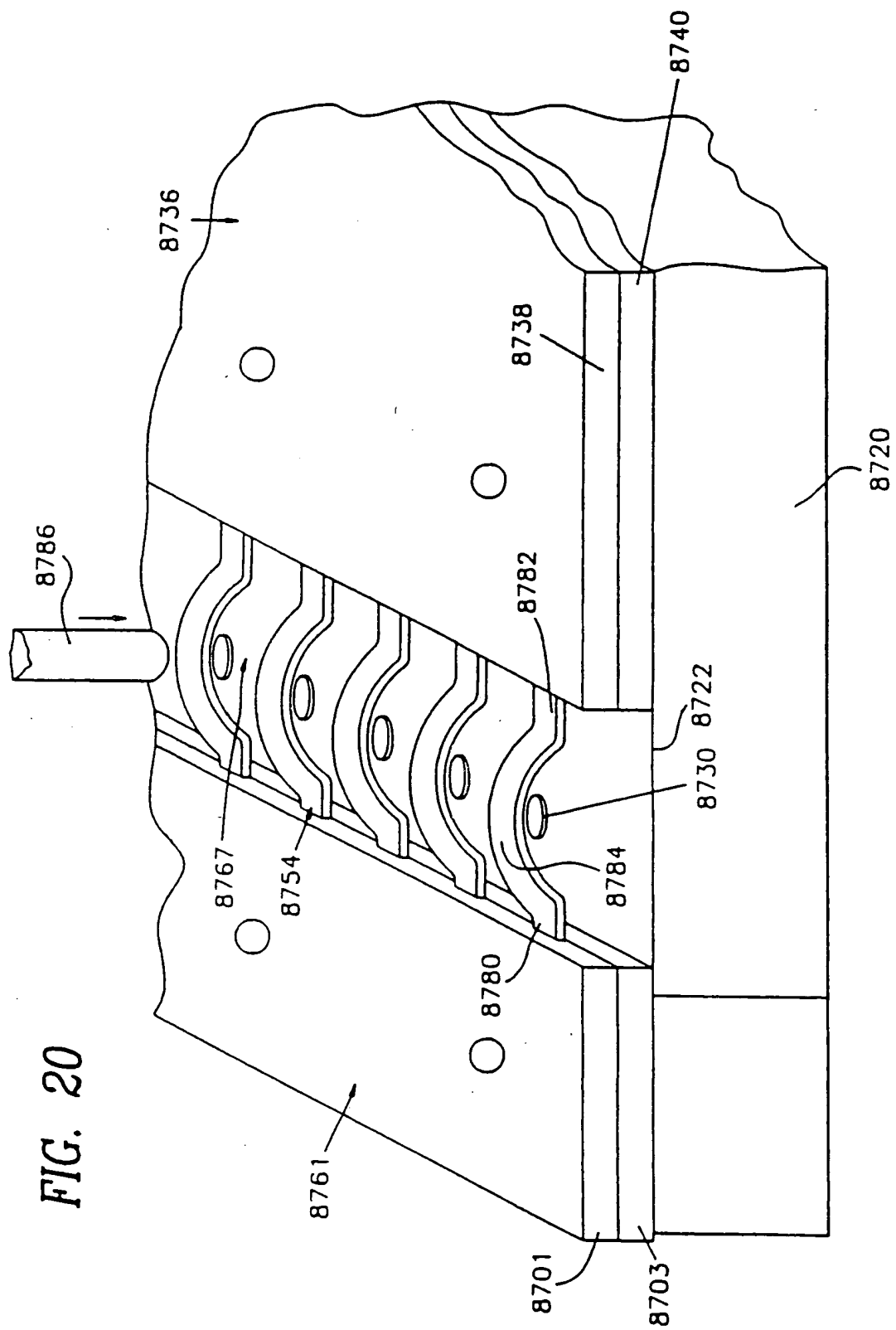


FIG. 21

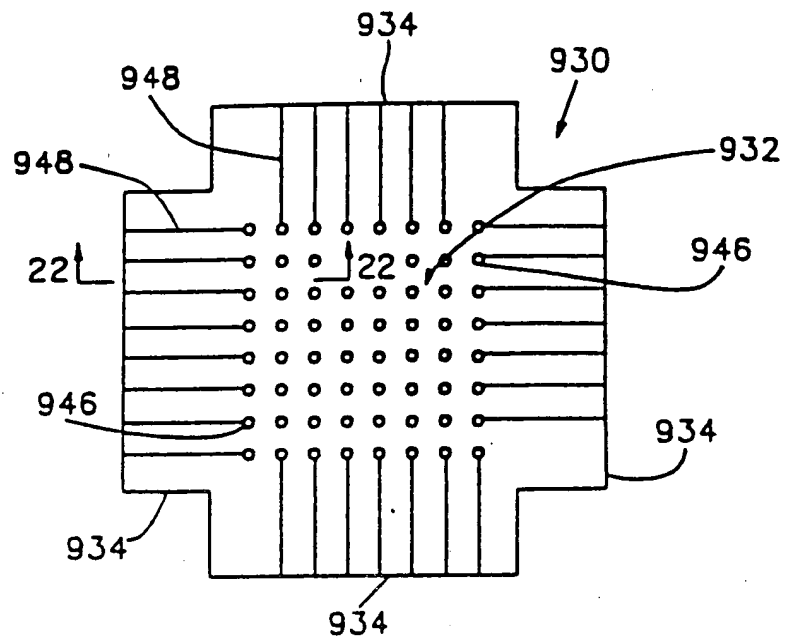


FIG. 22

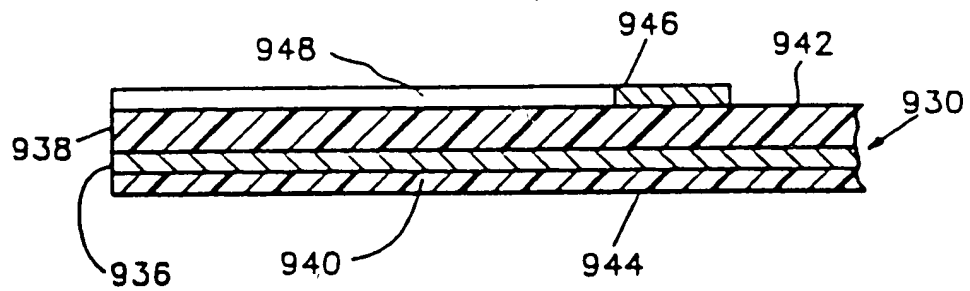


FIG. 23

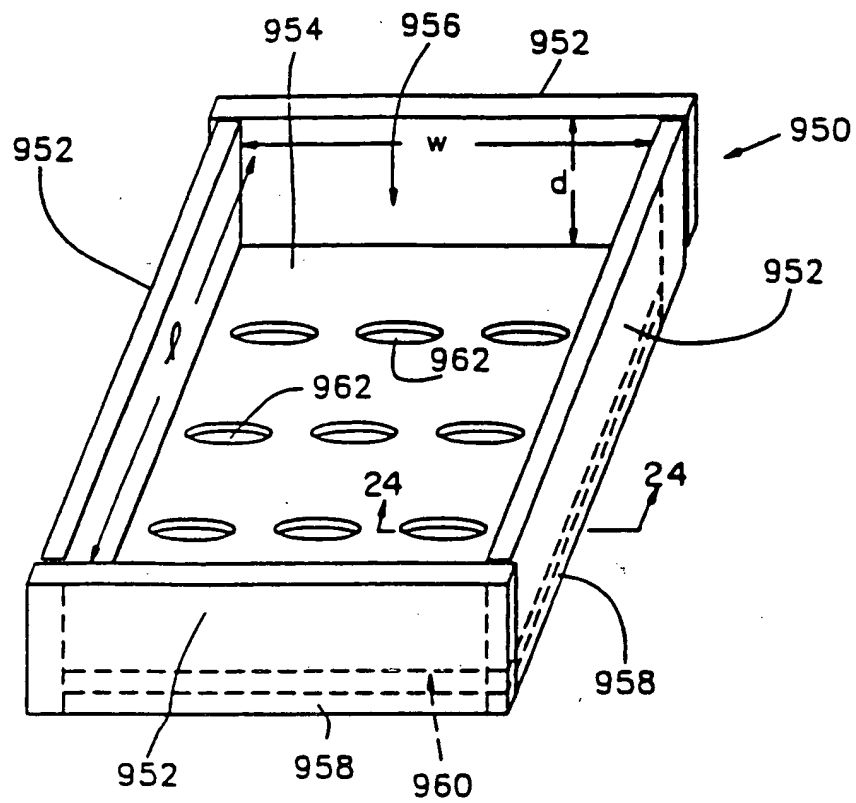


FIG. 24

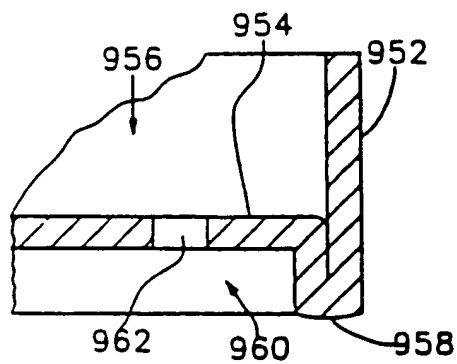


FIG. 25

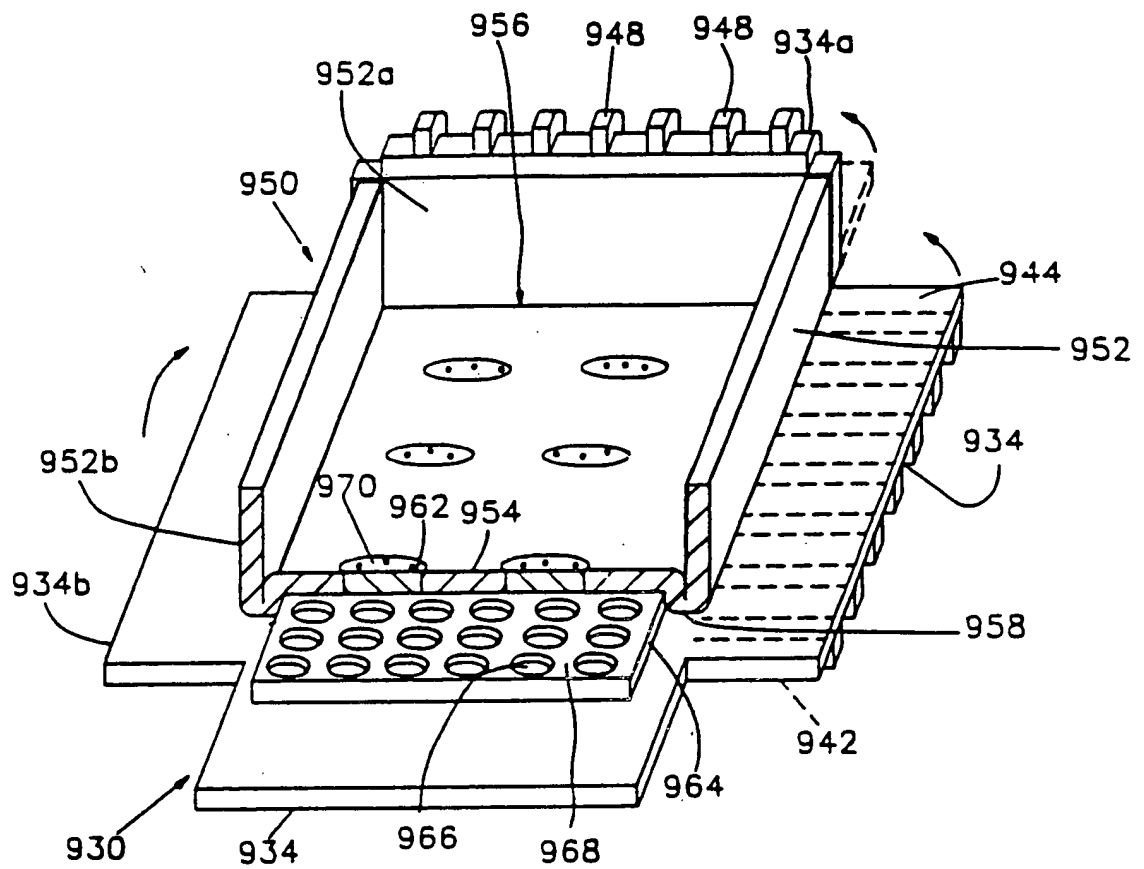
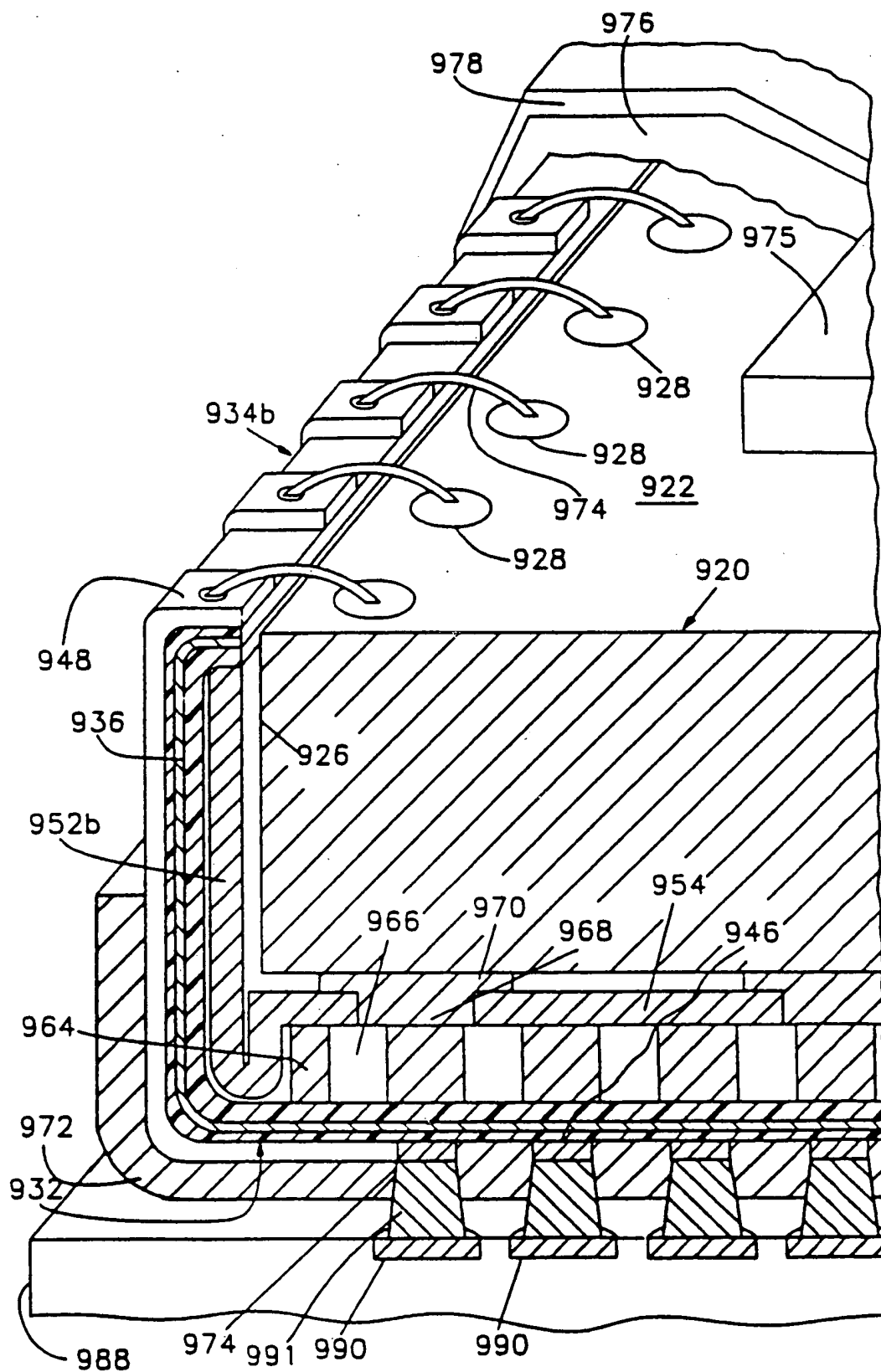


FIG. 26



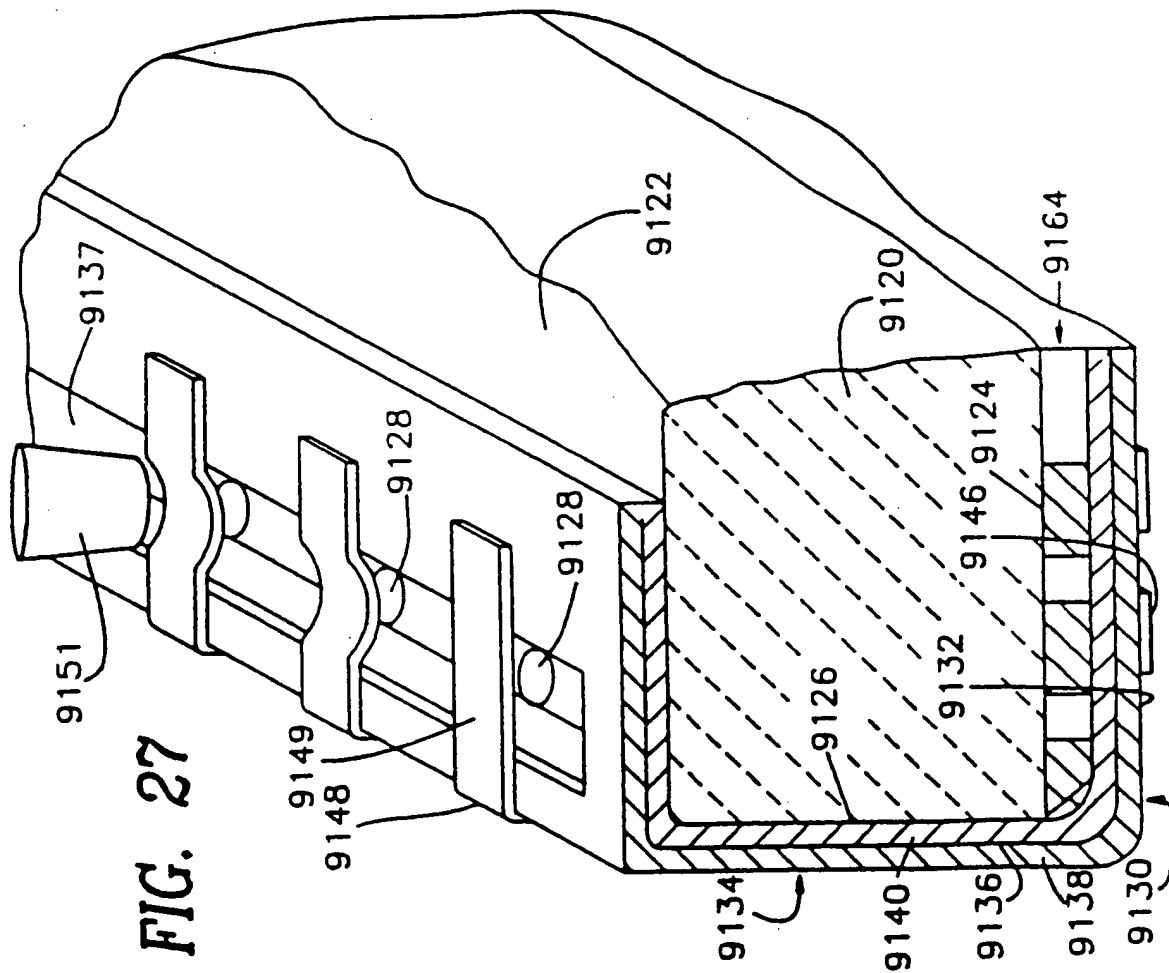


FIG. 27

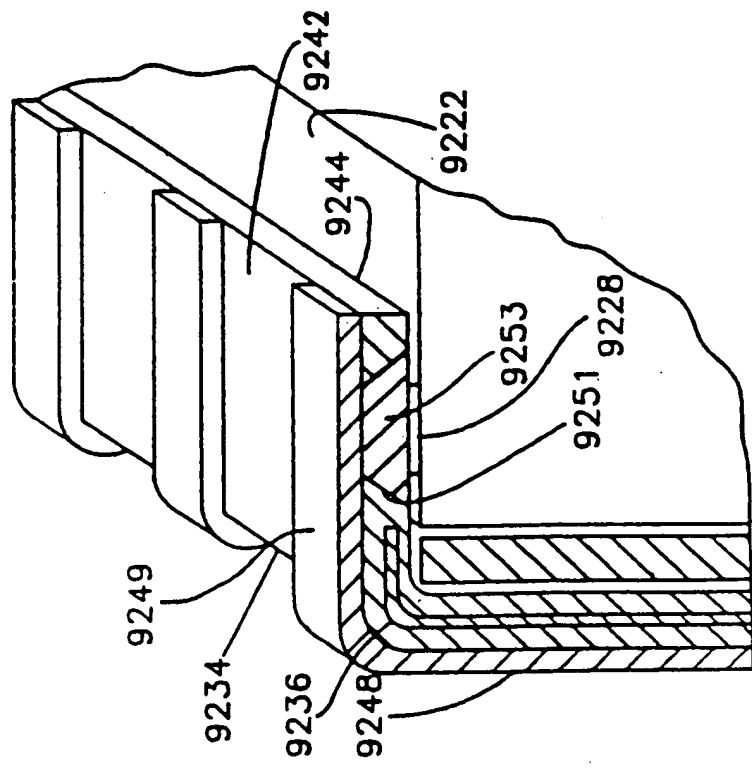
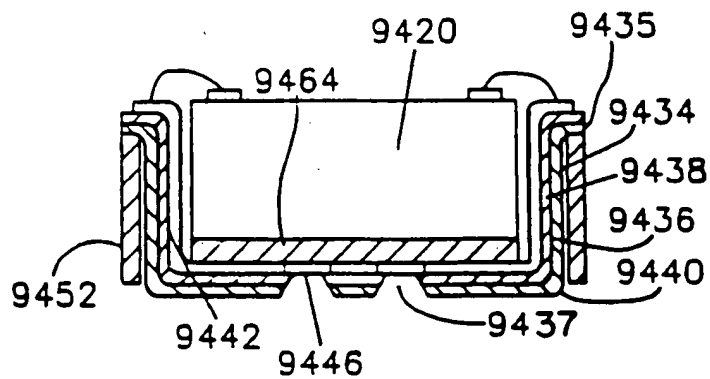
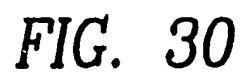


FIG. 28

This diagram shows a cross-sectional view of a multi-layered electronic assembly. The assembly consists of several stacked layers and components. At the top, a layer is labeled 9338. Below it is a component labeled 9377. A central vertical structure is labeled 9356. To the right of this central structure, a layer is labeled 9381. Below the central structure, a layer is labeled 9379. The main body of the assembly is a large rectangular block labeled 9320. Inside this block, there are several internal layers or components labeled 9328, 9383, and 9322. On the right side of the main block, there is a layer labeled 9324. Below the main block, there is a series of vertical structures labeled 9346 and 9395. At the bottom of the assembly, there is a base layer labeled 9391 and 9393.



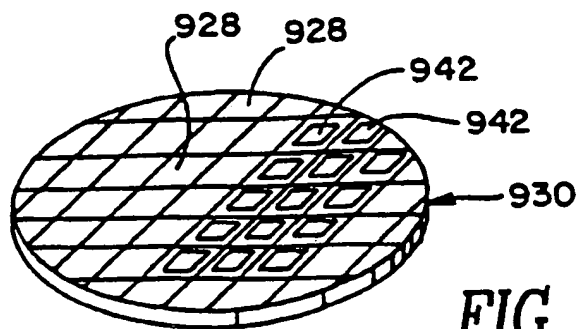


FIG. 31

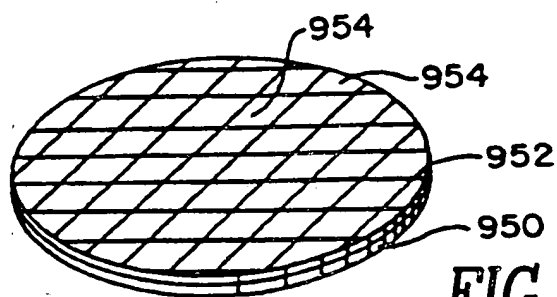


FIG. 32

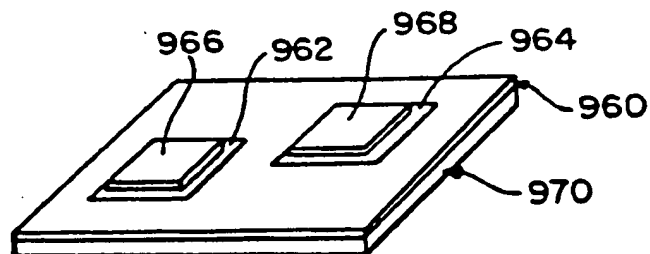


FIG. 33